Costas Argyrides, PhD, MBA, SMIEEE

CONTACT INFORMATION

Advanced Micro Devices (AMD),
2485 Augustine Dr., Mail Stop 2.161
Santa Clara, 95054,
California, USA

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Nationality: Cypriot

CURRENT ROLES

Advanced Micro Devices (AMD), Santa Clara, CA, USA.
Senior Member of Technical Staff (SMTS). GPU RAS Lead: 10/2015-Date
Advanced Micro Devices (AMD), Shanghai, China.
Senior Member of Technical Staff (SMTS). GPU RAS Lead: 03/2017-Date

- ❑ Responsible for the design/validation of the EDC part of the GPU. I have to work with other Architects and decide together which EDC technique will be applied in each part of the Graphics Core.
- ❑ Ensuring high RAS (Reliability/Availability/Serviceability) of the Graphics Core

European Commission, Brussels, Belgium.
Cyprus Ambassador for the European Pillar of Social Rights 10/2017-Date

- ❑ Working with European Commission and help raise awareness about the European Pillar of Social Rights

WORK EXPERIENCE

European Commission, Brussels, Belgium.
Cyprus Ambassador for the 2018 Vocational Skills Week 01/2018-01/2019
European Commission, Brussels, Belgium.
Cyprus Ambassador for the 2017 Vocational Skills Week 01/2017-01/2018

- ❑ Work with the European Commission and local VET Directorate to promote VET as a way to help young and adult learners discover their talents and as a smart choice that leads to high-quality jobs and increased employability.

Advanced Micro Devices (AMD) Gmbh, Munich, Deutschland.
Senior Member of Technical Staff (SMTS). Shader Core RAS DV lead: 11/2014-10/2015

- ❑ Responsible for the validation strategy of the EDC part of the Shader Core. I have to maintain the validation's test plan and ensure high quality of the validation strategy.
- ❑ Responsible for the design of the EDC part of the Shader Core. I have to work with the Architects and decide together which EDC technique will be applied in each part of the Shader Core.
- ❑ Design and apply tests to obtain the FIT of the proposed design.
- ❑ Ensuring high RAS (Reliability/Availability/Serviceability) of the Shader Core

Intel Barcelona, Validation Engineer: 11/2011-09/2014

- ❑ Validating the XEON Phi coprocessor.
- ❑ Planning the validation strategy for different features of the x86 architecture, guaranteing the quality of both the validation strategy and the coprocessor.
- ❑ Designing and developing tests to support the validation strategy.

- ❑ Running the tests, rooting the cause of malfunctions in the design if case they exist and reporting them.

Universitat Politecnica de Catalunya, Visiting Research staff: **11/2011-09/2014**
Working in the field of Reliable Computer Systems and System Validation.
Newcastle University, Visiting Research staff: **03/2011-03/2013**
Working in the field of reliable nanotechnology based circuits
Oxford Brookes University, Post-Doctoral Researcher: **05/2010 - 01/2011**
Working in the field of reliable and secure computer systems
University of Bristol, Post-Doctoral Researcher: **01/2009 - 03/2010**
Working in the field of embedded memories and Many-core Network-on-Chips
evolvI.T., Managing Director/Business Analyst: **09/2009-11/2014**

- ❑ Performing research in the area of fault tolerance and reliability. Consulting organizations and companies on how to improve their I.T. services by proposing innovative I.T. solutions and tool development in accordance to their needs.
- ❑ Negotiating and finalizing the design of the solution with the customers, then mediating it to the development team and monitor the whole process in order to meet the high standards required.
- ❑ Preparing reports for the customers/subcontractors.
- ❑ Assigning tasks to the group members and collaborating with each partner tracking weekly progress and sending reports to to the customers/subconstructors.
- ❑ Ensuring that all the project deadlines are met.

University of Cambridge, Visiting Fellow: **02/2008 - 08/2008**
Working on a DTI project at the University of Cambridge in the field of "Ultra Low-Power Micro-Hotplate Smart Gas-Sensor".
University of Warwick, Research Fellow: **02/2008 - 08/2008**
Working on an EPSRC project at the University of Warwick in the field of SOI Gas Sensors with title "Nano-structured micro-power smart gas sensors".
Georgia Institute of Technology (GA, USA), Visiting Fellow: **01/2006 - 03/2006**
Working with a group of students performing research on fault-tolerant and low power chip designs.

EDUCATION

Cyprus International Institute of Management (CIIM), Cyprus **03/2015 - 06/2018**
Masters of Business Administration (MBA)
Grade: Distinction
Dissertation title: Importing, Promoting and Distributing Novel Products in the Cyprus Market.
Dissertation Grade: 94%
Completed Courses: Financing of New Ventures, Business Ventures-From Idea to Execution, Communication Skills, Competitive Analysis, Corporate Finance, Digital Marketing, Ethics, CSR & Sustainability, Financial Accounting, International Business, Leadership, Managerial Economics, Managing Strategic Change, Marketing Management, Negotiating Skills, Organizational Behaviour, Presentation Skills, Starting a New Business, Strategic Marketing. Quantitative & Qualitative Methods
Fully funded by: Philelefthteros Newspaper.

University of Bristol, UK **10/2005 - 10/2008**
Ph.D. in Computer Science (Top 5 Universities in UK)
Thesis title: Novel Fault-Tolerant Techniques for the Improvement of Reliability and Yield in Advanced Technologies (I completed my PhD the 25^{th} month but due to the internal

regulations of the University of Bristol, I was not allowed to submit my thesis before the completion of the 33^{rd} month in the program).
Supervisor: Prof. Dhiraj K. Pradhan
Short Description: My thesis was completed in 6 parts.

- ❑ A novel multiple-error correcting technique.
- ❑ A novel SRAM memory design with improved reliability using Built-In-Current-Sensors.
- ❑ An innovative memory design to improve the fabrication yield while reducing the cost per chip.
- ❑ A framework to cope with the reliability and yield trade-off in nanotechnology based circuits.
- ❑ A multiple SEU tolerance FPGA.
- ❑ Algorithmic level fault tolerance technique to cope with long duration transients

Partially funded by: Department of Computer Science, University of Bristol, UK.

University of Bristol, UK **2004 - 2005**
M.Sc. in Computer Science (Top 5 Universities in UK)
Grade: Merit
Thesis title: A Novel Soft Error Tolerant Low Power RAM Architecture
Supervisor: Prof. Dhiraj K. Pradhan
Short abstract: We analyzed H-tree RAM architecture and we propose to incorporate on chip coding to protect against soft errors. It resulted in significant power savings of more than 50% and more than 34% decrease in delay over traditional RAM architecture while the reliability is significantly improved.
*Partially funded by:*MISYS foundation

Moscow Power Engineering Institute, Technical University(MPEI-TU), RU 2000 - 2004
B.Sc. Informatics and Computer Science (Top 3 Engineering Universities in Russia)
Grade: Distinction, 96%
Thesis: My thesis was completed in three parts:

- ❑ Using assembly language, I have programmed a Texas Instruments micro-controller to linearize the inputs (resistances) of a smart transmitter. The output(current) was transmitted up to 5km.
- ❑ Computerize a private institute. Created a database for student registration, attendances, fee payments and for the personnel files. A website was also designed and implemented. The institute was preparing 200 students for the university entering exams.
- ❑ Design a computer network for two offices in 1km distance with 20PC's. We had to prepare a tech report on the design of the network with all detailed information, for equipment and software that we needed for the implementation.

TEACHING EXPERIENCE

University of Bristol, Teaching and Learning in Higher Education course **12/2008**
Attended course for Teaching and Learning in Higher Education and certificate of completion obtained. The course aims to help all involved with teaching students become established and confident in their teaching.

University of Bristol, Teaching Assistant: **01/2009 - 06/2009**
Course "Fault Tolerant Computer Design (COMSM30125)". Offering tutorials, assessing assignments and marking tests for 12 students.

University of Bristol, Teaching Assistant: **10/2005 - 01/2008**
Course "Introduction to Computer Architecture (COMS M1302)". Offering tutorials, as-

sessing assignments and marking tests for more than 20 students.

University of Bristol, Teaching Assistant: **01/2006 - 06/2007**
Course "Fault Tolerant Computer Design (COMSM30125)". Offering tutorials, assessing assignments and marking tests for more than 20 students.

MPEI(TU), Lab Assistant: **09/2001 - 06/2003**
"Programming technology". Tutorials and marking of assignments and exams. More than 30 students in each lab session.

STUDENTS SUPERVISED

PhD

- **Nikolaos Mavrogiannakis, PhD candidate** , **10/2009 - 01/2013**
  University of the West of England (UWE), Bristol, Department of Computer Science
  Title: Hardware and Software Based Fault Tolerant Techniques for the Overall Improvement of System's Reliability

MSc

- **Kokkinos Costas, MSc**, **01/2011 - 10/2011**
  University of Bristol, Department of Computer Science
  Title: A framework to evaluate fault tolerant memories in advanced technologies

- **Dimosthenous Georgios, MSc candidate**, **01/2009 - 11/2009**
  University of Bristol, Department of Computer Science
  Title: A CAD tool for Synthesis and analysis of logic in nano-scale crossbars Architectures. Grade 79% (Rank #2 between 79 students)

- **Marinos Lemoniatis, MSc candidate**, **01/2007 - 9/2007**
  University of Bristol, Department of Computer Science
  Thesis Title: Novel techniques for minimization of MODDs. Grade 68%

PROFESSIONAL ACTIVITIES

Founding member of the Working Group for the Standardization of Reliability (Other members include IROC technologies, Hitachi, Uni. Of Newcastle, Nebrija University Spain, TIMA Labs France) - Reliability Information Interchange Format. The scope of the group is to **Create** a new IEEE standard for reliability.
Organizing Committee for the 1st workshop of the Working Group for the Standardization of Reliability, during DATE 2013.
Keynote speaker for the 14^{th} Latin American Test Workshop (IEEE LATW-2013)

Reviewer

- IEEE Transactions on Reliability
- IEEE Transactions on Nanotechnology
- IEEE Transactions on Devices and Materials Reliability
- IEEE Transactions on Computers
- IEEE Transactions on VLSI
- IEEE Transactions on CAS
- Design Automation Conference (DAC)
- Design Automation and Test in Europe (DATE)
- International On-Line Testing Symposium (IOLTS)
- Latin American Test Workshop (LATW)

GRANTS & AWARDS

- ❑ O1 Visa (It is awarded to an individual who possesses extraordinary ability), United States Citizenship and Immigration Services (USCIS). **08/2015**
- ❑ MBA Scholarship. Phileleftheros Newspaper. **02/2015**
- ❑ Intel's internal award for excellent performance. **10/2012**
- ❑ Travel Grant Award. Oxford Brookes University. **06/2010**
- ❑ Research Funding. Oxford Brookes University **01/2010**
- ❑ "Reliability Aware Yield Improvement Technique for Nanotechnology Based Circuits" appeared in the proceedings of the 22^{nd} annual symposium on Integrated circuits and system design SBCCI '09, Natal, Brazil, September 2009. **Best Paper Award**. **09/2009**
- ❑ Roberts fund. University of Bristol. **09/2009**
- ❑ ReMacore, Reliable Manycore Chips. Funded from Cyprus Research Promotion Foundation. I was a member of the consortium. **11/2008**
- ❑ Roberts fund. University of Bristol. **02/2008**
- ❑ International Travel Grant. Royal Academy of Engineering. **09/2007**
- ❑ Scholarship for doctoral studies. University of Bristol, Department of Computer Science. **07/2007**
- ❑ International Travel Grant. Royal Academy of Engineering. **03/2007**
- ❑ "A Fault Tolerant Multiplier less Decimation Filter" appeared in the proceedings of International Conference on Embedded Systems, Mobile Communication and Computing, Bangalore, India, August 2006. **Best Paper Award**. **08/2006**
- ❑ Scholarship. Misys Foundation. **03/2005**
- ❑ Top 10 students with excellent performance.Moscow Power Engineering Institute-Technical University **06/2004**

LIST OF PUBLICATIONS

Journals

2018

J.1. R. Gonzalez-Toral, P. Reviriego, J.A. Maestro **C. Argyrides**, J. Li "A Fast Technique to Reduce Power Consumption on Linear Block Codes Used to Protect Registers"*IEEE Transactions on Device and Materials Reliability*, In press

J.2. J. Li, P. Reviriego, L. Xiao, **C. Argyrides**, J. Li "Extending 3-bit Burst Error-Correction Codes With Quadruple Adjacent Error Correction"*IEEE Transactions on VLSI*, Volume 26, Issue 2, Page(s): 221 - 229, Feb. 2018

2013

J.3. **C. Argyrides**, P. Reviriego, J. A. Maestro, "Using single error correction codes to protect against isolated defects and soft errors"*IEEE Transactions on Reliability*, 62(1): 238-243 (2013).

2012

J.4. P. Reviriego, **C. Argyrides**, J. A. Maestro, "Efficient Error Detection in Double Error Correction BCH Codes for Memory Applications" *Microelectronics Reliability (ISSN: 0026-2714), 2012*, 52(7): 1528-1530 (2012).

2011

J.5. **C. Argyrides**, F. Vargas, D. K. Pradhan "Reliability Analysis of H-Tree RAM Memories Implemented with BICS and Parity Codes for Multiple-Bit Upset Correction" *IEEE Transactions on Reliability*, Volume 60, Issue 3, Page(s): 528-537, September 2011.

J.6. P. Reviriego, **C. Argyrides**, J. A. Maestro, D. K. Pradhan "Improving Memory Reliability against Soft Errors Using Block Parity " *IEEE Transactions on Nuclear Sciences*. Volume 58, Issue 3, Page(s) 981 - 986, June 2011.

J.7. P. Reviriego, **C. Argyrides**, J. A. Maestro, D. K. Pradhan "Fault Tolerant Single Error Correction Encoders" *Journal of Electronic Testing: Theory and Applications*. Volume 27, Issue 2, Pages 215-218, April 2011.

J.8. **C. Argyrides**, D. K. Pradhan, T. Kocak "Matrix Codes for Reliable and Cost Efficient Memory Chips" *IEEE Transactions on VLSI*,Volume: 19, Issue: 3, Pages 420-428, March 2011.

2010

J.9. **C. Argyrides**, P. Reviriego, D. K. Pradhan, J. A. Maestro "Matrix-Based Codes for Adjacent Error Correction" *IEEE Transactions on Nuclear Sciences*, Vol 57, no. 4, pages 2106 - 2111, Aug 2010.

2009

J.10. J Mathew, A Jabir, H. Rahaman, **C. Argyrides**, D. K. Pradhan, "On the Synthesis of Bit-Parallel Galois Field Multipliers with On-line SEC and DED."*International Journal of Electronics*

Refereed conferences and workshops proceedings

2018

C.11. H. Grigoryan, S. Shoukourian, G. Harutyunyan, Y. Zorian, **C. Argyrides**, "Advanced ECC-Based FIT Rate Mitigation Technique for Automotive SoCs", *IEEE International Test Conference (ITC)*, USA, 2018, Paper Auto 3.2, pp. 1-6.

2011

C.12. **C. Argyrides**, R. Fereira, C. A. Lisboa, L. Carro "Decimal Hamming: A Novel Software-Implemented Technique to Cope with Soft Errors" *26th IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems (DFT 2011)*, September 2011.

2010

C.13. P. Reviriego, **C. Argyrides**, J. A. Maestro and D. K. Pradhan "Enabling Performance versus Reliability Tradeoffs in Memories Using Block Parity" 11^{th} *European Conference on Radiation Effects on Components and Systems - RADECS 2010* September 20-24, Austria.

C.14. J. Fernando, N. Mavrogiannakis **C. Argyrides**,C. A. Lisboa, L. Carro "Multiple Bit Error Detection and Correction in Memory " *EUROMICRO Digital System Design*, September 2010.

C.15. N. Mavrogiannakis **C. Argyrides**, D. K. Pradhan "Improved Yield in Nanotechnology Circuits using Non-square Meshes" *IEEE Commputer Society Annual VLSI Symposium (ISVLSI 2010)*, July 2010.

C.16. Mavrogiannakis, N.**C. Argyrides**, Pradhan, D.K., "Improving reliability for bit parallel finite field multipliers using Decimal Hamming," Proceedings of *East-West Design & Test Symposium (EWDTS 2010)*, pp. 69-72, 17-20 September 2010.

C.17. **C. Argyrides**,C. A. Lisboa, D. K. Pradhan, L. Carro " Evaluation of a New Low Cost Software Level Fault Tolerance Technique to Cope with Soft Errors " *10th IEEE Latin-American Test Workshop (LATW 2010)*, March 2010.

2009

C.18. **C. Argyrides**, P. Reviriego, D. K. Pradhan and J. A. Maestro "A novel error correction technique for adjacent errors" 10^{th} *European Conference on Radiation Effects on Components and Systems - RADECS 2009* September 14-18 in Bruges, Belgium

C.19. **C. Argyrides**,C. A. Lisboa, D. K. Pradhan, L. Carro "Reliability Aware Yield Improvement Technique for Nanotechnology Based Circuits" 22^{nd} *annual symposium on Integrated circuits and system design SBCCI '09*, Natal, Brazil, September 2009. **(Best Paper Award)**

C.20. **C. Argyrides**,C. A. Lisboa, D. K. Pradhan, L. Carro "A Fast Error Correction Technique for Matrix Multiplication Algorithms" *Proceedings of IEEE International On-Line Testing Symposium (IOLTS 09)*, Lisbon, Portugal, 24-27 June, 2009

C.21. **C. Argyrides**,C. A. Lisboa, A. Al-Yamani, D. K. Pradhan, L. Carro "Increasing Memory Yield in Future Technologies through Innovative Design" *IEEE International Symposium on Quality Electronic Design (ISQED 09)*, 16-18, March 2009.

C.22. **C. Argyrides**,C. A. Lisboa, D. K. Pradhan, L. Carro "Single Element Correction in Sorting Algorithms with Minimum Delay Overhead" *10th IEEE Latin-American Test Workshop (LATW09)*, 2-5, March 2009.

C.23. **C. Argyrides**,C. A. Lisboa, D. K. Pradhan, L. Carro "Minimizing the Recomputation Time in Soft Error Tolerant Matrix Multiplication Algorithms" *At the 1st HiPEAC Workshop on Design for Reliability (DFR09)*, 25, Jan 2009.

C.24. **C. Argyrides**, D. K. Pradhan "Multiple Event Upsets Aware FPGAs Using Protected Schemes" *Daghstul proceedings for 2009*.

2008

C.25. **C. Argyrides**, H.R. Zarandi and D. K. Pradhan "Multiple SEU Tolerance in LUTs of FPGAs Using Protected Schemes" *8th European Workshop on Radiation Effects on Components and Systems (RADECS08)*, September 2008.

C.26. **C. Argyrides**, F. Vargas, D. K. Pradhan "Embedding Current Monitoring in H-Tree RAM Architecture for Multiple SEU Tolerance and Reliability Improvement" *Proceedings of IEEE International On-Line Testing Symposium (IOLTS 08)*, Rhodes, Greece, 3-6 July 2008

C.27. **C. Argyrides**, S. Loizidou-Himona, D. K. Pradhan "Area Reliability tradeoff in Improved Reed Muller Coding"*Proceedings of SAMOS VIII workshop*, in Samos, Greece, July 21-24, 2008

C.28. **C. Argyrides**, S. Loizidou-Himona, D. K. Pradhan "Yield Improvement and Power Aware Low Cost Memory Chips"*Workshop on Radiation Effects and Fault Tolerance in Nanometer Technologies at Computing Frontiers 2008*, Ischia, Italy, May 2008

C.29. C. A. Lisboa, **C. Argyrides**, D. K. Pradhan, L. Carro "Algorithm Level Fault Tolerance: a Technique to Cope with Long Duration Transient Faults in Matrix Multiplication Algorithms" *Proceedings of VLSI Test Symposium (VTS 08)*, April, 2008

C.30. **C. Argyrides**, F. Vargas, D. K. Pradhan "Merging Built-in Current Sensor with H-Tree Architecture for SRAM Reliability Improvement" *Proceedings of IEEE Latin American Test Workshop 2008 (LATW 08)*, Puebla Mexico, February 2008

C.31. J. Mathew, **C. Argyrides**, A. M Jabir, D. K. Pradhan "Single Error Correcting Finite Field Multipliers over GF(2m)" *Proceedings of 21st Conference on VLSI Design (VLSI 08)*, Hyderabad, India, 4-8 Jan 2008

2007

C.32. **C. Argyrides**,C. A. Lisboa, D. K. Pradhan, L. Carro "Working at Algorithm Level to Minimize Recomputation Time when Coping with Long Duration Transients", *Proceedings of the 1st International Workshop on Dependable Circuits Design*, Buenos Aires, Argentina, December. 2007

C.33. **C. Argyrides**, D. Pradhan "Improved Decoding Algorithm for High Reliable Reed Muller Coding," *20th IEEE International System On Chip Conference (SOCC 2007)*,September 2007.

C.34. **C. Argyrides**, A. A. Al-Yamani, D. K. Pradhan "High Defect Tolerant Low Cost Memory Chips," *20th IEEE International System On Chip Conference (SOCC 2007)*, September 2007.

C.35. **C. Argyrides**, H. Zarandi, D. K. Pradhan "Matrix Codes: Multiple Bit Upsets Tolerant Method for SRAM Memories," *22nd IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems (DFT'07)*, September 2007.

C.36. **C. Argyrides**, D. K. Pradhan "Novel Soft Error Robust Power Aware Memory Designs" *International IEEE East West Design and Test Symposium (EWDTS 07),* Yerevan, Armenia, 7-10 September 2007.

C.37. **C. Argyrides**, D. K. Pradhan "Yield Improvement for High Defect Rate Nanotechnology Circuits" *International IEEE East West Design and Test Symposium (EWDTS 07),* Yerevan, Armenia, 7-10 September 2007.

C.38. **C. Argyrides**, C. Lisboa, L. Carro, D. K. Pradhan "A Novel Soft Error Tolerant Low Power RAM Architecture" in . 20^{th} *annual symposium on Integrated circuits and system design SBCCI '07*, September 2007.

C.39. **C. Argyrides**, D. K. Pradhan "Highly Reliable Power Aware Memory Design," *IEEE International On-Line Testing Symposium 2007 (IOLTS)*, July 2007.

C.40. **C. Argyrides** "High Defect Tolerant Robust Memory Designs," *DSN Student Forum*, June 2007.

C.41. H.R. Zarandi, S.G. Miremadi, **C. Argyrides**, D. K. Pradhan "CLB-based Detection and Correction of Bit-flip faults in SRAM-based FPGAs," *Proceedings of IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2007.

C.42. **C. Argyrides**, H.R. Zarandi, D. K. Pradhan "Multiple Upsets Tolerance in SRAM Memory," *Proceedings of IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2007.

C.43. H.R. Zarandi, S.G. Miremadi, **C. Argyrides**, D. K. Pradhan "Online Detection and Correction of Soft-Errors in LUTs of SRAM-based FPGAs," *Proceedings of European Test Symposium (ETS)*, May 2007.

C.44. **C. Argyrides**, H.R. Zarandi, D. K. Pradhan "Efficient Method to Tolerate Multiple Bit Upsets in SRAM Memory," *Proceedings of European Test Symposium (ETS)*, May 2007.

C.45. **C. Argyrides**, D. K. Pradhan "Fast Reed Muller Decoding for Multi-Bit Upset Aware Memory Designs," *Proccedings of Latin American Test Workshop (LATW)*, March 2007.

C.46. **C. Argyrides**, S. Ramsundar , A. Al-Yamani, D. K. Pradhan "Non-square Meshes for Improved Yield in Nanotechnology Circuits," *Proccedings of Latin American Test Workshop*, March 2007.

C.47. H.R. Zarandi, S.G. Miremadi, **C. Argyrides**, D. K. Pradhan "Fast SEU Detection and LUT Configuration Bits of SRAM-based FPGAs," *Proceedings of 14th IEEE Reconfigurable Architecture Workshop, in associated with IPDPS*, March 2007.

2006

C.48. **C. Argyrides**, A. Al-Yamani, D. K. Pradhan "Performance Analysis of an Error Tolerant Low Power Memory Architecture," *IEEE International Design and Test Workshop*, Dubai, November 2006.

C.49. A.J. Bijoy, R. J. Babita, S. Juothish, **C. Argyrides**, J. Mathew "A Fault Tolerant Multiplier less Decimation Filter" *International Conference on Embedded Systems, Mobile Communication and Computing,* August 4th -5th 2006, Bangalore, India. **(Best Paper Award)**

PROFESSIONAL ACTIVITIES & MEMBERSHIPS

Senior Member IEEE
Member IEEE Reliability society
Member IEEE Computer society
Member IEEE Circuits and Systems (CAS) society
RIIF, Funding Member of Reliability Information Interchange Format. A work group for the standardization of the reliability
Funding member of the Systemic Approach research group.
Funding member of the Lemesos' research center. A non-profitable organization to support independent research in the area of Limassol, Cyprus. (Under development).

COMPUTING SKILLS

EDA tools:
Virtuoso (Cadence), Analog Artist (Cadence), HSPICE (Synopsis), PSPICE (Cadence), Microwind.
HDL tools:
VHDL, Verilog.
Programming Languages:
Turbo Pascal, C Programming language, Matlab, x86 Assembly language, LaTeX, HTML, CSS, Perl, shell scripting.
Operating Systems:
DOS, Windows 9x/XP/Vista, Unix, Linux.

LANGUAGES

Greek: native language.
English: (read, spoken, written) fluent.
Russian:(read, spoken) good command.